



# Product Change Notification

**Change Notification #:** 116783 - 00  
**Change Title:** Intel® Cyclone®V Devices, PCN 116783-00, Documentation, Data Sheet Update  
**Date of Publication:** February 26, 2019

## Key Characteristics of the Change:

Documentation

## Forecasted Key Milestones:

<b>Date Customer Must be Ready to Receive Post-Conversion Material:</b>	February 26, 2019
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## Description of Change to the Customer:

Intel is notifying customers of a documentation update for Cyclone V devices. The announcement went out to customers already under ADV1831.

The minimum Data Hold time ( $t_{DH}$ ) timing specification for Active Serial (AS) configuration scheme has been updated.

**Table 1: Minimum  $t_{DH}$  Specification**

Speed Grade	Change From	Change To		
		Commercial Grade (0C)	Industrial Grade (-40C)	Automotive Grade (-40C)
-6	2.5ns	2.3ns	N/A	N/A
-7	2.9ns	2.7ns	2.9ns	2.9ns
-8	2.9ns	2.7ns	2.9ns	N/A

The  $t_{DH}$  spec is stipulated in Table 60 of the datasheet. Please review the revision history for all other updates to the datasheet. The Cyclone V device datasheet can be found here:

<https://www.intel.com/content/www/us/en/programmable/documentation/mcn1422497163812.html>

## Customer Impact of Change and Recommended Action:

Customers should review their board design against the updated Cyclone V minimum  $t_{DH}$  spec, otherwise configuration may fail.

Customers can calculate the hold time required for Active Serial configuration scheme, as mentioned in the 'Evaluating Data Setup and Hold Timing Slack' section of AN822 to evaluate the hold time slack on the board. AN822 can be found here:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an822.pdf>

Additionally, Intel PSG will be introducing new packages, designated by new available OPNs (Ordering Part Numbers) with the “QS” suffix to support a reduced  $t_{DH}$  requirement. The current OPNs will still be available to support customers using parallel and partial reconfiguration modes or designs that meet the updated  $t_{DH}$  specification.

**Table 2**

Product Family	New Packages	Engineering Samples Available for Order
Cyclone V	U324, U484, F484, F672, F896, F1152	Q2 2019
Cyclone V SoC	U484, U672, F896	Q2 2019

For more information regarding the new package introduction, contact your local sales representative.

### Products Affected / Intel Ordering Codes:

All Cyclone V and Cyclone V SoC Devices

The list of affected OPNs can be downloaded in Excel form:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv1831-opn-list.xlsx>

### PCN Revision History:

**Date of Revision:**

February 26, 2019

**Revision Number:**

00

**Reason:**

Originally Published PCN



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**Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.**

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